RF Circuit Performance Degradation Due to Soft Breakdown and Hot-Carrier Effect in Deep-Submicrometer CMOS Technology

Qiang Li, *Student Member, IEEE*, Jinlong Zhang, Wei Li, *Student Member, IEEE*, Jiann S. Yuan, *Senior Member, IEEE*, Yuan Chen, *Senior Member, IEEE*, and Anthony S. Oates

***Abstract*—A systematic study of RF circuit performance degradation subject to oxide soft breakdown (SBD) and hot-carrier (HC) stress is presented in this paper. DC and RF characteristics before and after stress are extracted from the experimental data. The effects of SBD and HC stress on s-parameters, cutoff frequency, third-order interception point, and noise parameters are examined. The performance drifts of gain, noise figure, linearity, and input matching of the RF low-noise amplifier are demonstrated by SpectreRF simulation results based on measured device data.**

***Index Terms*—CMOS, constant voltage stress, hot carriers, low-noise amplifier, power amplifier, scattering parameters, soft breakdown.**

I. Introduction

DUE TO continued scaling, deep-submicrometer CMOS transistors could produce a cutoff frequency (f_T) over 70 GHz and a noise figure (NF) lower than 0.5 dB [1]. These features are more and more attractive for RF application up to 5 GHz [2], [3]. CMOS technologies also offer low-cost and high-integration capability. However, hot-carrier (HC) stress and soft-breakdown (SBD)-induced device degradation pose a limit to the device scaling. Moreover, transistor aging and SBD induced degradation will seriously reduce the design margin of the RF circuits. It is important to understand the impact of stress on RF circuit performance using deep-submicrometer processes.

Gate oxide breakdown and the HC effect are two critical issues of deep-submicrometer CMOS device and circuit reliability [4]. The performance drifts due to HC stress could be examined by the transconductance degradation, threshold voltage, and mobility shift. The increased random thermal motion of carriers in the channel after HC stress increases the channel thermal noise, a critical factor in low-noise-amplifier design. Compared with hard breakdown (HBD), SBD becomes more prevalent for thinner oxides and for oxide stress at relatively lower voltages [5]. Moreover, HC injection triggers more SBD in addition to conventional Fowler–Nordheim (FN) injection [6].

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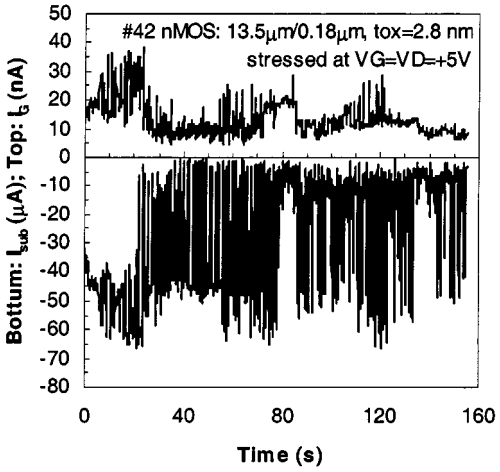

Fig. 1. Gate and substrate currents versus time.

In this paper, typical RF parameters such as cutoff frequency f_T, maximum frequency of oscillation $f_{\max}$, and noise factors ($F_{\min}, R_n, G_{\rm opt}$, and $B_{\rm opt}$) subject to SBD and HC stress are studied. Gain, NF, linearity, and s-parameters of a CMOS low-noise amplifier (LNA) using 0.18- and 0.16-μm CMOS technologies are evaluated.

II. Experimental Evidence of HC and SBD

When the oxide is scaled down to a 2-nm regime, SBD would take place before HBD. SBD, however, has not been commonly recognized to degrade device and circuit characteristics. In this paper, experimental evidence of the impact of SBD (along with the HC injection) on the RF circuits is presented.

The devices used are 0.18- and 0.16-μm CMOS transistors. The gate oxide thicknesses are 2.8 and 2.4 nm, respectively. The wafers are tested with the Cascade 12000 Probe Station and Agilent 4156B Semiconductor Parametric Analyzer for dc measurements, while the RF experiments up to 50 GHz are carried out using the Agilent 8510C Network Analyzer. Oxide stress and channel HC effects are applied to the transistor simultaneously to mimic the circuit operation condition while the source and body are grounded. The HBD voltage for this configuration is determined to be 5.7 V from voltage ramps for 0.18-μm

TABLE I
KEY BSIM3v3 PARAMETERS OBTAINED FROM EXPERIMENTS

Parameters	V_{th0}	K_1	V_{sat}	μ_0	V_{off}	*N-factor*	P_{clm}
% change	11.7	100.2	-84	-68.8	163.3	-31.4	-96.8

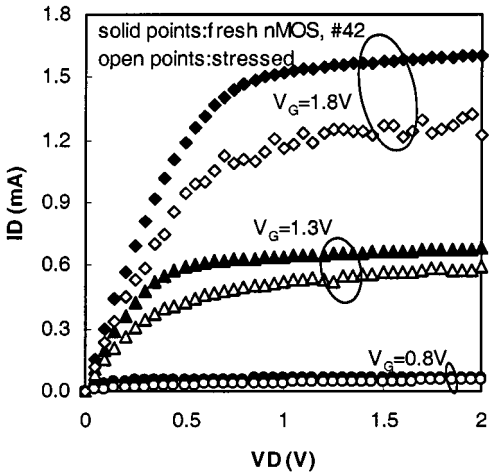

Fig. 2. Measured drain current versus drain–source voltage at $V_{\rm GS} = 0.8, 1.3$, and 1.8 V.

2.8-nm oxide nMOSFET. The accelerated stress condition is then carefully set at $V_G = V_D = 5$ V. A typical time-dependent dielectric breakdown (TDDB) result is shown in Fig. 1. In this figure, many SBD events take place in the gate and substrate currents. One observes that the HC injection triggers more SBD occurrences. The drain current decreases due to the electron trapping and interface state generation as the degradation percentage goes up. The drain current shows considerable depress, as evidenced in Fig. 2. Electron trapping may result in the increase of threshold voltage, while the interface state generation could decrease the electron mobility in the channel. The device dc parameters before and after the stress are extracted using BSIMpro. The key device parameters extracted from experiments are summarized in Table I.

Fig. 3 shows the measured transconductance g_m as a function of $V_{\rm GS}$ before and after stress. The transconductance is degraded over the entire saturation region. S-parameters are measured in the common source–bulk configuration for 0.16 μm ($t_{\rm ox} = 2.4$ nm) devices. On-wafer dummy structures are used to calibrate the pad parasites. Since the transistors in RF applications are usually biased in the saturation region, the RF performance at $V_{\rm GS} = 0.85$ V and $V_{\rm DS} = 1.5$ V is characterized. Fig. 4 shows the effect of the stress on the forward transmission scattering parameter (S_{21}). The magnitude of S_{21} decreases as the stress time increases. The decrease of S_{21} is consistent with the degradation of the transconductance. It is interesting to note from Fig. 5 that the reverse transmission gain S_{12} only decreases slightly, while the input reflection coefficient S_{11} is changed significantly, as shown in Fig. 6. The large change of S_{11} may attributed to the significant degradation of the gate capacitance $C_{\rm gs}$ and transconductance g_m. For the output reflection coefficient S_{22}, the change is not noticeable. All measured dc and RF parameters are transported into SPICE model files and an .s2p file for RF circuit simulation using Cadence SpectreRF.

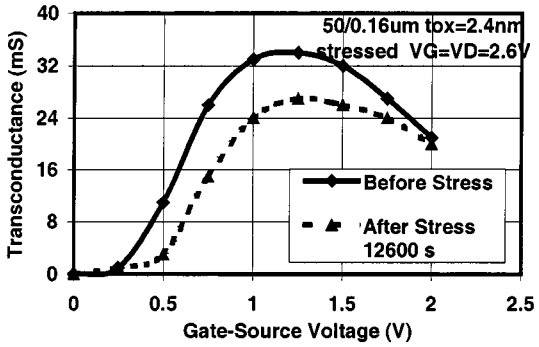

Fig. 3. Transconductance versus gate–source voltage measured at $V_{\rm DS} = 1.5$ V before and after stress.

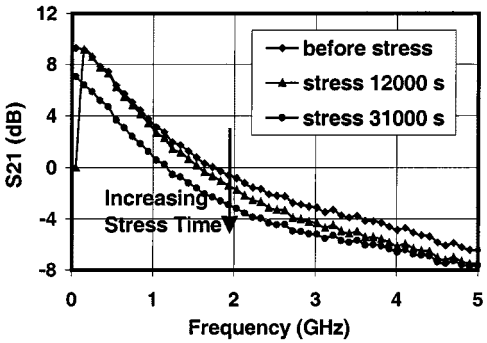

Fig. 4. Measured S_{21} versus frequency (fresh device, stressed after 12 000 and after 31 000 s).

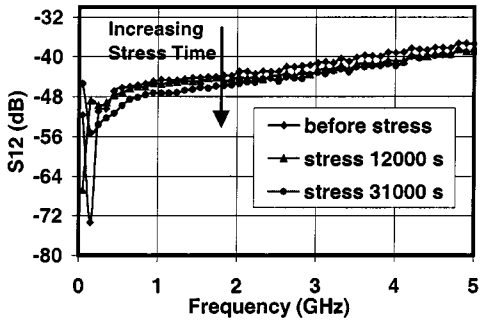

Fig. 5. Measured S_{12} versus frequency (fresh device, stressed after 12 000 and 31 000 s).

III. DEGRADATION OF RF PARAMETERS

The important parameters considered here are gate resistance, threshold voltage, mobility, transconductance, and parasitic capacitances. The impact of these parameters on the cutoff frequency f_T is expressed as

$$f_T = \frac{3}{2}\frac{\mu_{\rm eff}}{L^2}(V_{\rm gs} - V_T)\frac{L\varepsilon_{\rm sat} + \dfrac{V_{\rm gs} - V_T}{2}}{(L\varepsilon_{\rm sat} + V_{\rm gs} - V_T)^2} \qquad (1)$$

where $\varepsilon_{\rm sat} = 2v_{\rm sat}/\mu_{\rm eff}$.

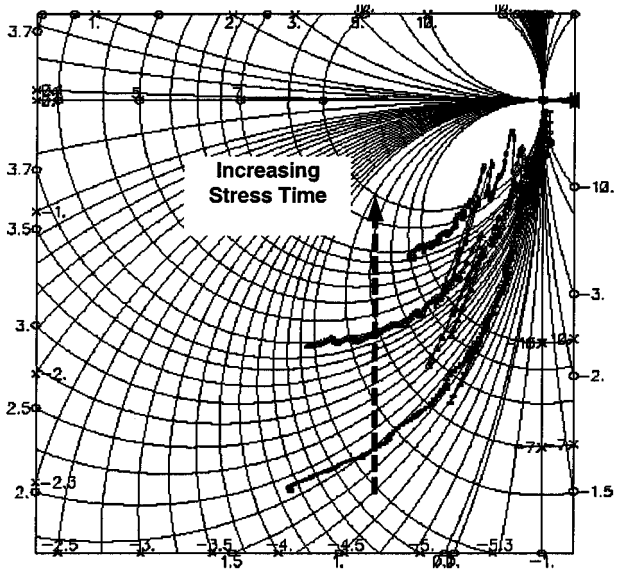

Fig. 6. Measured S_{11} versus frequency as a function of stress time.

The maximum oscillation frequency $f_{\max}$ is approximated by [7]

$$f_{\mathrm{MAX}} \cong \sqrt{\frac{f_T}{8\pi R_g C_{\mathrm{gd}}}}. \tag{2}$$

The noise performance is usually characterized by the following four noise parameters [8]:

$$\mathrm{NF} = \mathrm{NF}_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{\mathrm{opt}})^2 + (B_s - B_{\mathrm{opt}})^2\right] \tag{3}$$

where $\mathrm{NF}_{\min}$ is the minimum NF that a circuit can achieve with the optimum source admittance condition $(G_s = G_{\mathrm{opt}}, B_s = B_{\mathrm{opt}})$. R_n determines the sensitivity of the NF when G_s and B_s differ from G_{opt} and B_{opt}. Expressions for the four noise parameters include the effect of gate resistance and are derived and summarized in Table II [9].

The input third-order intermodulation power P_{IIP3} is given as

$$P_{\mathrm{IIP3}} = \frac{M^2}{2R_S} = \left|\frac{2A_1(s)}{3A_3(s_1, s_2, s_3)R_S}\right| \tag{4}$$

where $A_1(s), A_3(s_1, s_2, s_3)$ are Volterra series coefficients of the circuit. These coefficients are a function of $g_m, C_{\mathrm{gs}}, \omega_T$, operation frequency ω, and circuit components (L_g, L_s, and R_s). Since g_m, C_{gs}, and ω_T are changed after SBD and HC stress, RF circuit performances are thus degraded after stress [10]. Measured s-parameters are converted into admittance y-parameters, and the intrinsic device characteristics are calculated using a deembedded technology. In Fig. 7, the measured degradation of cutoff frequency versus stress time is displayed. It is clear from Fig. 7 that the cutoff frequency decreases rapidly at the initial stage of stress and then saturates at much longer stress time. An LNA operated at 2.45 GHz is simulated using measured 0.16-μm device s-parameters. Fresh s-parameter results are compared with two sets of stressed ones, as shown in Fig. 8. With the increase of stress time, the magnitude of S_{21} is reduced and the input impedance matching degrades at the center frequency.

TABLE II
EQUATIONS FOR NOISE PARAMETERS

Noise parameter	*Expression*
NF_{min}	$1+2\frac{f}{f_T}\sqrt{\frac{\delta(1-\lvert c\rvert^2)}{5}\left[\gamma'\left(1+\frac{f}{f_T}R_g g_m\right)^2+\frac{g_m^2}{g_{d0}}R_g\right]}$
R_n	$\frac{\gamma' g_{d0}}{g_m^2}(1+\omega C_{gs}R_g)^2 + R_g$
G_{opt}	$\sqrt{\frac{\delta\omega^2 C_{gs}^2(1-\lvert c\rvert^2)}{5\frac{\gamma' g_{d0}}{g_m^2}(1+\omega C_{gs}R_g)^2+5g_{d0}R_g}}$
B_{opt}	$\frac{\omega C_{gs}\sqrt{\gamma' g_{d0}}}{\sqrt{\gamma' g_{d0}(1+\omega C_{gs}R_g)^2+R_g g_m^2}}+\frac{g_m}{g_{d0}(1+\omega C_{gs}R_g)}\lvert c\rvert\sqrt{\frac{\delta}{5\gamma'}}\omega C_{gs}$

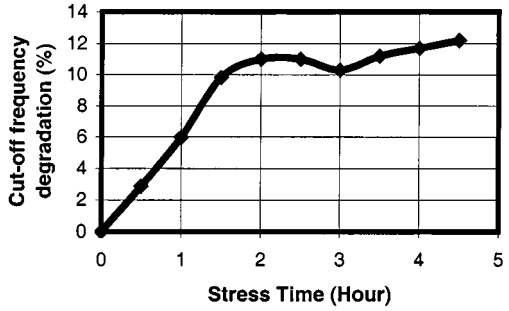

Fig. 7. Measured cutoff frequency degradation versus stress time.

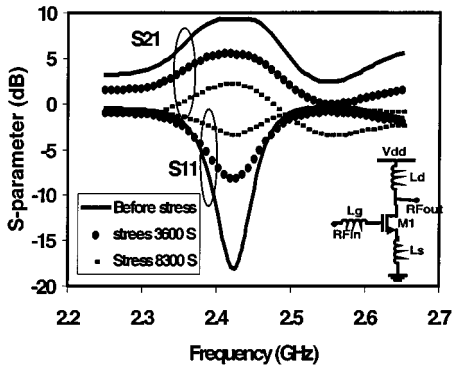

Fig. 8. S_{21} and S_{11} versus frequency of a single transistor LNA before and after stress.

IV. RF Circuit Performance Degradation

RF circuit performances such as the NF, gain, impedance matching, and linearity (third-order intermodulation point and 1-dB compression point) are evaluated using the 0.18-μm device parameters before and after stress. Fig. 9 shows the schematic of a CMOS RF LNA under test at 2.4 GHz. The differential architecture is selected for better noise rejection of common-mode interference. The gate inductor L_g and on-chip spiral inductor L_s are used for the input impedance matching. The drain inductor L_d is used to get the maximum power gain. A cascoded second stage reduces the Miller effect and improve the output–input isolation. The transistors of the circuit are operated in the saturation region with an effective gate voltages $|V_{G,\mathrm{eff}}| = |V_{\mathrm{GS}} - V_t|$ of several 100 mV and the drain voltages of several 100 mV. With the change of the input signal level, the drain–source voltages of transistors M1–M5 may be high

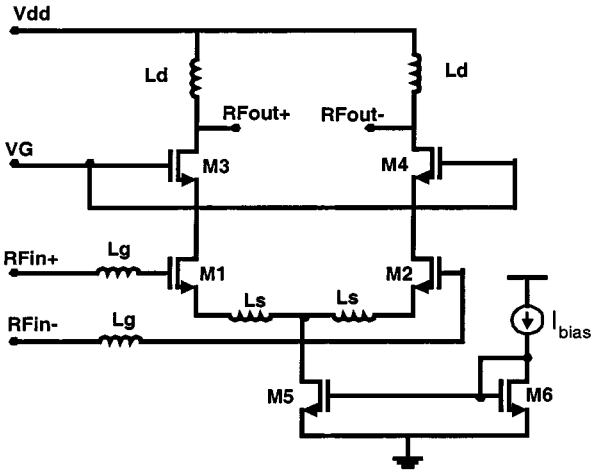

Fig. 9. Schematics of a CMOS LNA.

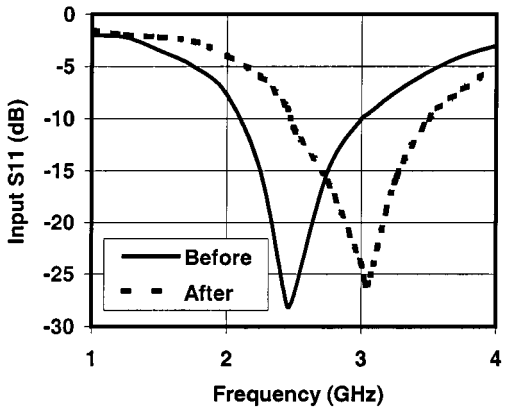

Fig. 10. S_{11} versus frequency before and after stress.

enough to induce a hot electron effect. The diode connection M6 has a fixed $V_{\rm DS} = V_{\rm GS}$. Therefore, M6 is not affected by HCs. The MOS transistor model used is the RF simulation is BSIM3v3.

Fig. 10 shows S_{11} versus frequency before and after stress. The dc stress applied is at $V_{\rm GS} = 5$ V and $V_{\rm DS} = 5$ V for 155 s. In Fig. 10, the minimum S_{11} position has been moved away from 2.45 GHz by 600 MHz after stress. At 2.45 GHz, S_{11} is changed from -27 to -9 dB. Fig. 11 shows the NF degradation of the LNA subject to stress. At 2.45 GHz, the NF of the LNA is increased from 2 to 3 dB. The fluctuations of carriers in the transistor channel current causes noise at the gate electrode. This increases the NF of the circuit. Fig. 12 displays the voltage gain versus frequency. The voltage gain is reduced by 5 dB around the center frequency. Fig. 13 compares the output spectra of the LNA before and after stress. The third-order intermodulation to first–order term (3IM/1ST) ratio of the LNA before stress is -50 dBc, while it is -18 dBc after stress. The linearity property is degraded after stress. Table III summarizes the RF performance degradation of the LNA under stress. For the common-source input stage of the LNA, the single-ended input impedance is

$$Z_{\rm in} = \frac{1}{j\omega C_{\rm gs}} + j\omega(L_s + L_g) + g_m \frac{L_s}{C_{\rm gs}}. \qquad (5)$$

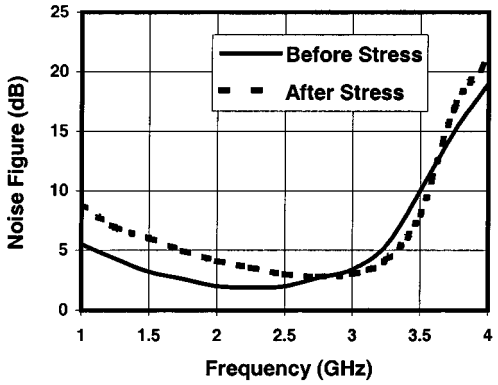

Fig. 11. NF versus frequency before and after stress.

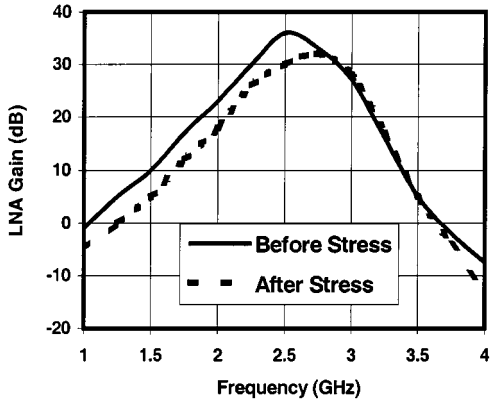

Fig. 12. Voltage gain versus frequency before and after stress.

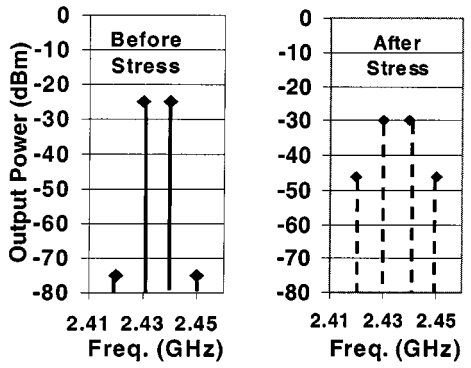

Fig. 13. Two-tone simulation before and after stress.

From the above equation, the degradation of g_m and the drift of $C_{\rm gs}$ after stress change both the real and imaginary parts of the input impedance. The mismatch causes S_{11} to shift away from the designed center frequency. The NF is degraded because of a reduction of f_T and the derivation of impedance from its optimum value. Since $\text{Gain} = Q_{\rm in} g_m R_L$, both the degradation of the input stage $Q_{\rm in}$ and g_m can be attributed to the decrease of gain.

In conjunction with HC degradation, the gate oxide breakdown is an important reliability issue for the design of power amplifiers (PAs). Since the PA handles a relatively large signal, both oxide and channel electrical fields can be very high. The output power and power efficiency could be degraded due to HC and SBD stress. Examine Fig. 14 for typical operating points of

TABLE III
RF PERFORMANCE DEGRADATION OF A DIFFERENTIAL LNA UNDER STRESS

Condition	*NF(dB)*	*Gain(dB)*	*3IM/1ST (dBc)*	*S_{11}(dB) @2.45GHz*
Before stress	**2**	**36**	**-50**	**-27**
After stress	**3**	**31**	**-18**	**-9**

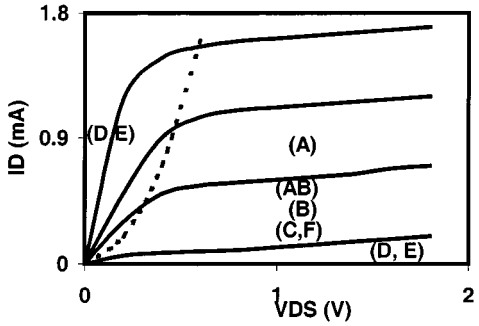

Fig. 14. Typical operating points of different PAs.

PAs. Classes A, B, AB, C, and F are biased in the saturation region. The order of the oxide stress from $V_{\rm GS}$ for those classifications is A $>$ AB $>$ B $>$ C, F in standby. The peak drain–source voltage is about 2 $V_{\rm DD}$ to cause HC degradation. The transistors in classes D and E PAs are operated ideally as a switch in either the zero voltage or zero current region. When the transistor is operated at the zero drain voltage region, the device suffers significant gate oxide stress. On the other hand, when the transistor is operated at the zero current region, the device suffers significant channel HC stress due to a very large drain voltage. The peak drain–source voltage for a class-E PA can be as high as 3.6 $V_{\rm DD}$. This gives considerable HC and gate oxide stress (due to the drain–gate overlap region stress [11]) to degrade PA performance. More experimental and design studies are ongoing at the University of Central Florida (UCF), Orlando.

V. SUMMARY

The impact of SBD and HC stress on the CMOS RF lower noise amplifier has been examined in detail using 0.18- and 0.16-μm CMOS technologies. HC aging reduces the drain current, transconductance, cutoff frequency, and S_{21} of the MOS transistors. Consequently, the gain, NF, third-order intermodulation, and s-parameters of the RF LNA show significant performance degradation. After accelerated stress at 5 V for 155 s, S_{11} is changed from -27 dB to -9 dB, LNA gain is degraded by 5 dB, NF increases from 2 to 3 dB, and 3IM/1ST ratio moves from -50 to -18 dBc at the designed frequency of 2.45 GHz.

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Yuan Chen (S'97–A'98–SM'99), photograph and biography not available at time of publication.

Anthony S. Oates, photograph and biography not available at time of publication.